AMENDMENTS TO THE CLAIMS

The following listing of the claims replaces any and all prior listings:

1. (Previously Presented) A semiconductor integrated circuit device, comprising:

a first internal circuit including a first metal-oxide semiconductor (MOS) transistor operating at a first voltage higher than a power supply voltage of the device;

a second internal circuit including a second MOS transistor operating at a second voltage lower than the first voltage;

restricting means for restricting a voltage transmitted from the first internal circuit to the second internal circuit; and

wherein the restricting means includes a third MOS transistor having a relatively thin gate insulation layer and operating at the second voltage, the voltage from the first internal voltage is applied to the second internal circuit through the third MOS transistor, and the second MOS transistor is controlled by a row address signal in a memory device.

2. (Original) The device of claim 1, wherein

the first MOS transistor has a relatively thick gate insulation layer,

the second MOS transistor has a relatively thin gate insulation layer, and

the voltage transmitted from the first internal circuit to the second internal voltage reduces an electric field applied to the gate insulation layer of the second MOS transistor.

3. (Original) The device of claim 1, wherein

the power supply voltage is an external power supply voltage for the device or an internal power supply voltage of the device, and

the second voltage is one of the power supply voltage, a voltage lower than the power supply voltage, and a voltage between the power supply voltage and the first voltage.

4. (Cancelled)

5. (Currently Amended) The device of claim 4 1, further comprising:

an inverter coupled to a connection node of the second and third MOS transistors, wherein the inverter drives a word line in the memory device.

6. (Currently Amended) The device of claim 5, wherein the inverter includes PMOS and NMOS transistors, each PMOS or NMOS transistor operating at a second voltage higher than the power supply voltage and having a relatively thick gate insulation layer.

7. (Cancelled)

8. (Currently Amended) The device of claim 7 1, further comprising:

an inverter coupled to a connection node of the second and third MOS transistors, wherein the inverter drives a word line in the memory device.

9. (Currently Amended) The device of claim 8, wherein the inverter includes PMOS and NMOS, each PMOS or NMOS transistor operating at a second voltage higher than the power supply voltage and having a relatively thick gate insulation layer.

10. (Currently Amended) A semiconductor integrated circuit device, comprising:

a power terminal receiving a high voltage that is higher than a power supply voltage of the device;

a first transistor having a drain coupled to the power terminal, a source coupled to the ~~first~~ high voltage, and a gate coupled to a first input signal;

a second transistor having a drain coupled to the power terminal, a source, and a gate coupled to a low voltage that is lower than the first high voltage; and

a third transistor having a drain coupled to the source of the second transistor, a source coupled to a ground voltage, and a gate coupled to a second input signal,

wherein the first transistor has a relatively thick gate insulation layer, and the second and third transistors each have a relatively thin gate insulation layer, and the second input signal includes a row address signal from a memory device.

11. (Previously Presented) The device of claim 10, wherein

the power supply voltage is an external power supply voltage for the device or an internal power supply voltage of the device, and

the low voltage is one of the power supply voltage, a voltage lower than the power supply voltage, and a voltage between the power supply voltage and the high voltage.

12. (Previously Presented) The device of claim 10, wherein the first input signal is selectable as one of a high level of the high voltage and a low level of the ground voltage.

13. (Previously Presented) The device of claim 10, wherein the second input signal is selectable as one of a high level of the low voltage and a low level of the ground voltage.

14. (Cancelled)

15. (Currently Amended) The device of claim ~~14~~ 10, further comprising:

an inverter coupled to a connection node of the second and third transistors, wherein the inverter drives a word line of the memory device.

16. (Currently Amended) The device of claim 15, wherein the inverter includes PMOS and NMOS transistors, each PMOS or NMOS transistor operating at a first voltage higher than the power supply voltage and having a relatively thick gate insulation layer.

17. (Original) The device of claim 10, further comprising:

a fourth transistor coupled between the third transistor and the ground voltage, wherein the fourth transistor has a relatively thin gate insulation layer.

18. (Currently Amended) The device of claim 17, wherein the fourth transistor is controlled by a block selecting signal from ~~a~~ the memory device.

19. (Currently Amended) A semiconductor integrated circuit device, comprising:

a power terminal receiving a high voltage higher than a power supply voltage of the device;

a first MOS transistor coupled between the power terminal and a first internal node;

a second MOS transistor coupled between the power terminal and a second internal node,

a third MOS transistor having a relatively thin gate insulation layer coupled between the first internal node and a third internal node ~~having a relatively thin gate insulation layer~~;

a fourth MOS transistor having a relatively thin gate insulation layer coupled between the second internal node and a fourth internal node ~~having a relatively thin gate insulation layer~~;

a fifth MOS transistor coupled between the third internal node and a ground voltage, the fifth MOS transistor controlled by a first input signal, and the first input signal includes a row address signal and a block selecting signal from a memory device; and

a sixth MOS transistor coupled between the fourth internal node and the ground voltage, the sixth MOS transistor controlled by an inverted version of the first input signal.

20. (Previously Presented) The device of claim 19, wherein

the first MOS transistor and the second MOS transistor each have a relatively thick gate insulation layer, and

the fifth MOS transistor and sixth MOS transistor each have a relatively thin gate insulation layer,

21. (Previously Presented) The device of claim 19, wherein

the power supply voltage is an external power supply voltage for the device or an internal power supply voltage of the device.

22. (Original) The device of claim 19, wherein the first MOS transistor is controlled by a voltage of the second internal node, and the second MOS transistor is controlled by a voltage of the first internal node.

23. (Previously Presented) The device of claim 19, wherein gates of the third and fourth MOS transistors are coupled to a low voltage that is lower than the high voltage.

24. (Previously Presented) The device of claim 23, wherein

the power supply voltage is an external power supply voltage for the device or an internal power supply voltage of the device, and

the low voltage is one of the power supply voltage, a voltage lower than the power supply voltage, and a voltage between the power supply voltage and the high voltage.

25. (Cancelled)

26. (Currently Amended) The device of claim ~~25~~ 19, wherein the first input signal and its inverted version are selectable to have one of a high level of the second low voltage and a low level of the ground voltage.

27. (Cancelled)

28. (Currently Amended) The device of claim ~~27~~ 19, wherein the first internal node is coupled to a row decoder and driver block of the memory device, and the row decoder and driver block selectively drives word lines of the memory device in response to row address signals.

29. (Currently Amended) The device of claim ~~25~~ 28, wherein

the row decoder and driver block includes a plurality of row decoder and driver circuits, each row decoder and driver circuit corresponding to a given word line, and

each row decoder and driver circuit further including:

a seventh MOS transistor having a source coupled to the high voltage, a drain coupled to a fifth internal node, and a gate connected to receive a second input signal; and

eighth and ninth MOS transistors serially coupled between the fifth internal node and the ground voltage,

wherein each of the seventh and eighth MOS transistors ~~have~~ has a relatively thick gate insulation layer, and the ninth MOS transistor has a relatively thin gate insulation layer; and

wherein the eighth MOS transistor is controlled by a voltage of the first internal node.

30. (Currently Amended) The device of claim 29, further comprising:

an inverter coupled to each of the corresponding fifth internal node, wherein the inverter drives ~~a~~ the corresponding word line of each of the row and driver circuit ~~the memory device~~.

31. (Currently Amended) The device of claim 30, wherein the inverter includes PMOS and NMOS transistors, each PMOS or NMOS transistor operating at a first voltage higher than the power supply voltage and having a relatively thick gate insulation layer.

32. (Currently Amended) A circuit device, comprising:

a first internal circuit including a first MOS transistor that has a relatively thick gate insulation layer operating at a first voltage that is higher than a power supply voltage of the device;

a second internal circuit operating at a second voltage that is lower than the first voltage;

an interface circuit restricting a voltage transmitted from the first internal circuit to the second internal circuit;

wherein the interface circuit includes a third MOS transistor operating at one of the first voltage and second voltage and having a relatively thin gate insulation layer and operating at the second voltage, the voltage from the first internal circuit being applied to the second internal circuit through the third MOS transistor, and the second internal circuit includes a second MOS transistor that has a relatively thin gate insulation layer, the second MOS transistor being controlled by a row address signal in a memory device.

33. (Currently Amended) The circuit de vice of claim 32, wherein

~~the first internal circuit includes a first MOS transistor that has a relatively thick gate insulation layer,~~

~~and~~

the voltage transmitted from the first internal circuit to the second internal voltage reduces an electric field applied to the gate insulation layer of the second MOS transistor.

34. (Cancelled)

35. (Previously Presented) The device of claim 33, wherein the interface circuit includes a third MOS transistor having a relatively thin gate insulation layer, the voltage from the first MOS transistor being applied to the second MOS transistor through the third MOS transistor.

~~35~~ 36. (Currently Amended) The device of claim ~~34~~ 32, wherein the third MOS transistor prevents the first voltage higher than the power supply voltage from being directly applied to the drain of the second MOS transistor, enabling the second MOS transistor to have the relatively thin gate insulation layer.

~~36~~ 37. (Currently Amended) The device of claim ~~34~~ 32, wherein the third MOS transistor reduces a gate-drain voltage of the second MOS transistor to alleviate the electric field applied to the gate insulation layer of the second MOS transistor.